

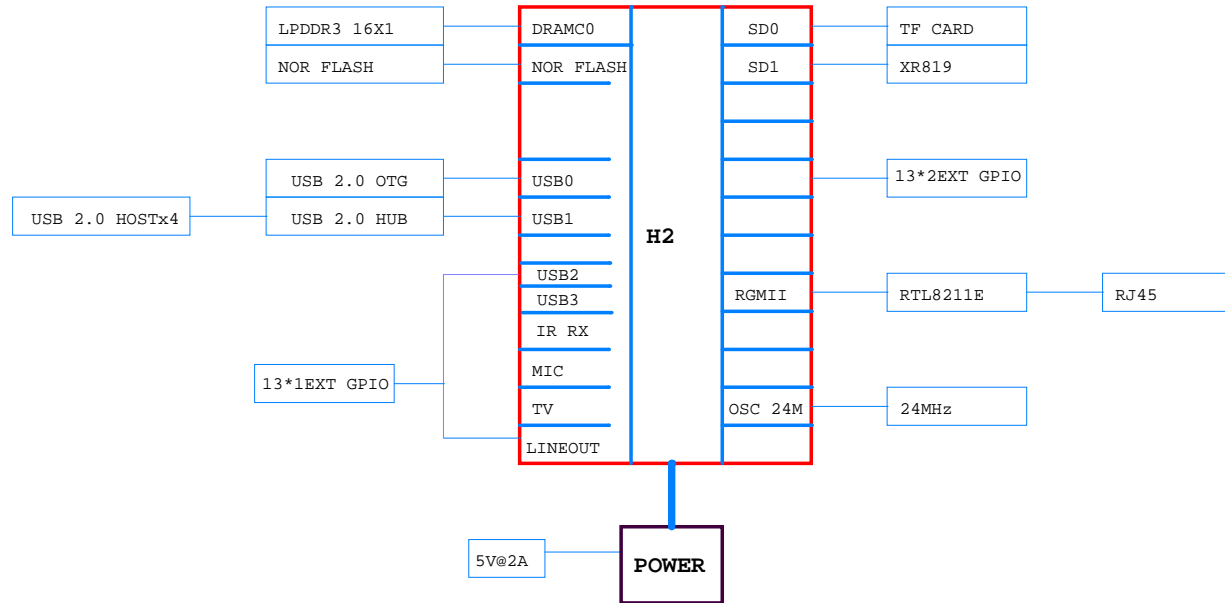
REVISION HISTORY

Schematics Index:

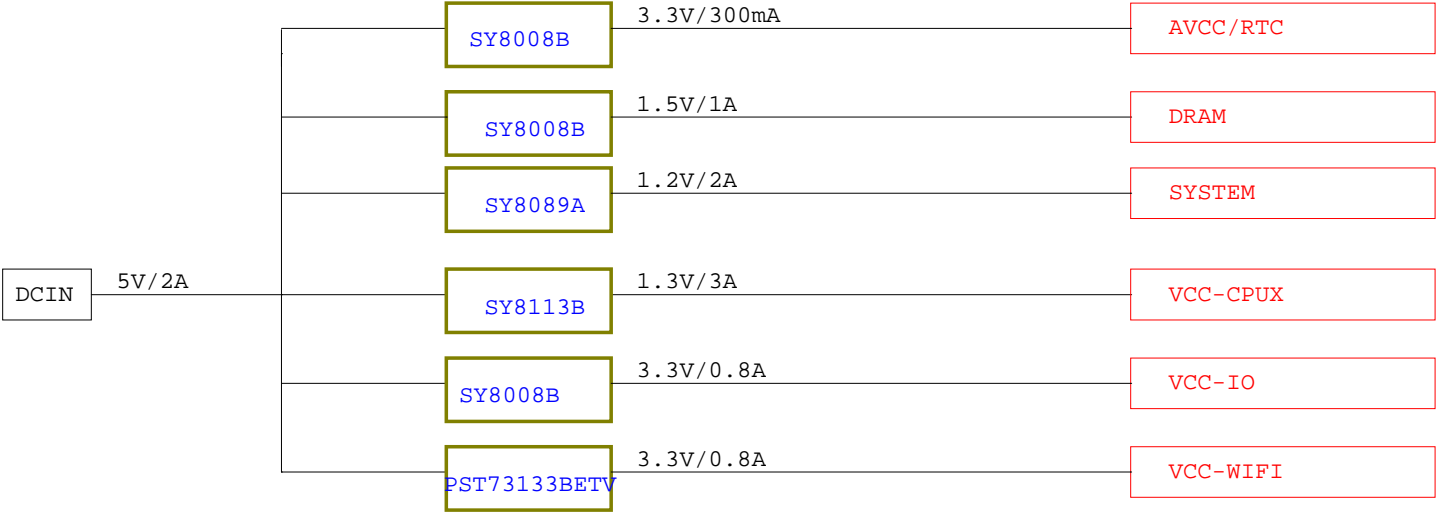
Revision	Description	Date	Drawn	Checked
Ver 1.0	Initial	2016-09-05		

- 1、WIFI更改为R189ETV
- 2、增加千兆网口
- 3、删除USB
- 4、百兆网口更改为内置变压器

BLOCK



POWER TREE



GPIO ASSIGNMENT

PIN	Define	CFG	Function
PA0	RMS/DRVVBUS0	3/1	JTAG /USB
PA1	TCK/DRVVBUS1	3/1	
PA2	TDO/WPS	3/1	
PA3	TDI	3	UART
PA4	JART-TX	3	
PA5	JART-RX	3	
PA6	NC	7	
PA7	NC	7	
PA8	NC	7	
PA9	NC	7	
PA10	NC	7	
PA11	NC	7	
PA12	NC	7	
PA13	NC	7	
PA14	NC	7	
PA15	STATUS-LED	1	LED
PA16	MUTE	1	AV
PA17	SPDIF-OUT	2	SPDIF
PA18	NC	7	
PA19	NC	7	
PA20	NC	7	
PA21	NC	7	

PIN	Define	CFG	Function
PC0	NWE	2/3	NAND /eMMC /NOR
PC1	NALE	2/3	
PC2	NCLE	2/3	
PC3	NCE1	2/3	
PC4	NCE0	2	
PC5	NRE	2/3	
PC6	NRB0	2/3	
PC7	NRB1	2	
PC8	NDQ0	2/3	
PC9	NDQ1	2/3	
PC10	NDQ2	2/3	
PC11	NDQ3	2/3	
PC12	NDQ4	2/3	
PC13	NDQ5	2/3	
PC14	NDQ6	2/3	
PC15	NDQ7	2/3	
PC16	NDQS	2/3	

PIN	Define	CFG	Function
PD0	NC	7	
PD1	NC	7	
PD2	NC	7	
PD3	NC	7	
PD4	NC	7	
PD5	NC	7	
PD6	NC	7	
PD7	NC	7	
PD8	NC	7	
PD9	NC	7	
PD10	NC	7	
PD11	NC	7	
PD12	NC	7	
PD13	NC	7	
PD14	NC	7	
PD15	NC	7	
PD16	NC	7	
PD17	NC	7	

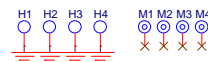
PIN	Define	CFG	Function
PE0	NC	7	
PE1	NC	7	
PE2	NC	7	
PE3	NC	7	
PE4	NC	7	
PE5	NC	7	
PE6	NC	7	
PE7	NC	7	
PE8	NC	7	
PE9	NC	7	
PE10	NC	7	
PE11	NC	7	
PE12	NC	7	
PE13	NC	7	
PE14	NC	7	
PE15	NC	7	

PIN	Define	CFG	Function
PF0	D1	2	CARD0
PF1	D0	2	
PF2	CLK	2	
PF3	CMD	2	
PF4	D3	2	
PF5	D2	2	
PF6	DET	0	

PIN	Define	CFG	Function
PG0	NC	7	
PG1	NC	7	
PG2	NC	7	
PG3	NC	7	
PG4	NC	7	
PG5	NC	7	
PG6	NC	7	
PG7	NC	7	
PG8	NC	7	
PG9	NC	7	
PG10	NC	7	
PG11	NC	7	
PG12	NC	7	
PG13	NC	7	

PIN	Define	CFG	Function
PL0	TWI	2	TWI
PL1	TWI	2	
PL2	USB0-DRVVBUS	1	USB
PL3	USB1-DRVVBUS	1	
PL4	RECOVERY	0	KEY
PL5	VCC-IO-EN	1	IO-EN
PL6	NC	7	WIFI-EN
PL7	WIFI-EN	7	
PL8	PWR-STB	1	
PL9	PWR-DRAM	1	
PL10	PWR-LED	1	
PL11	IR-RX	2	

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CPU

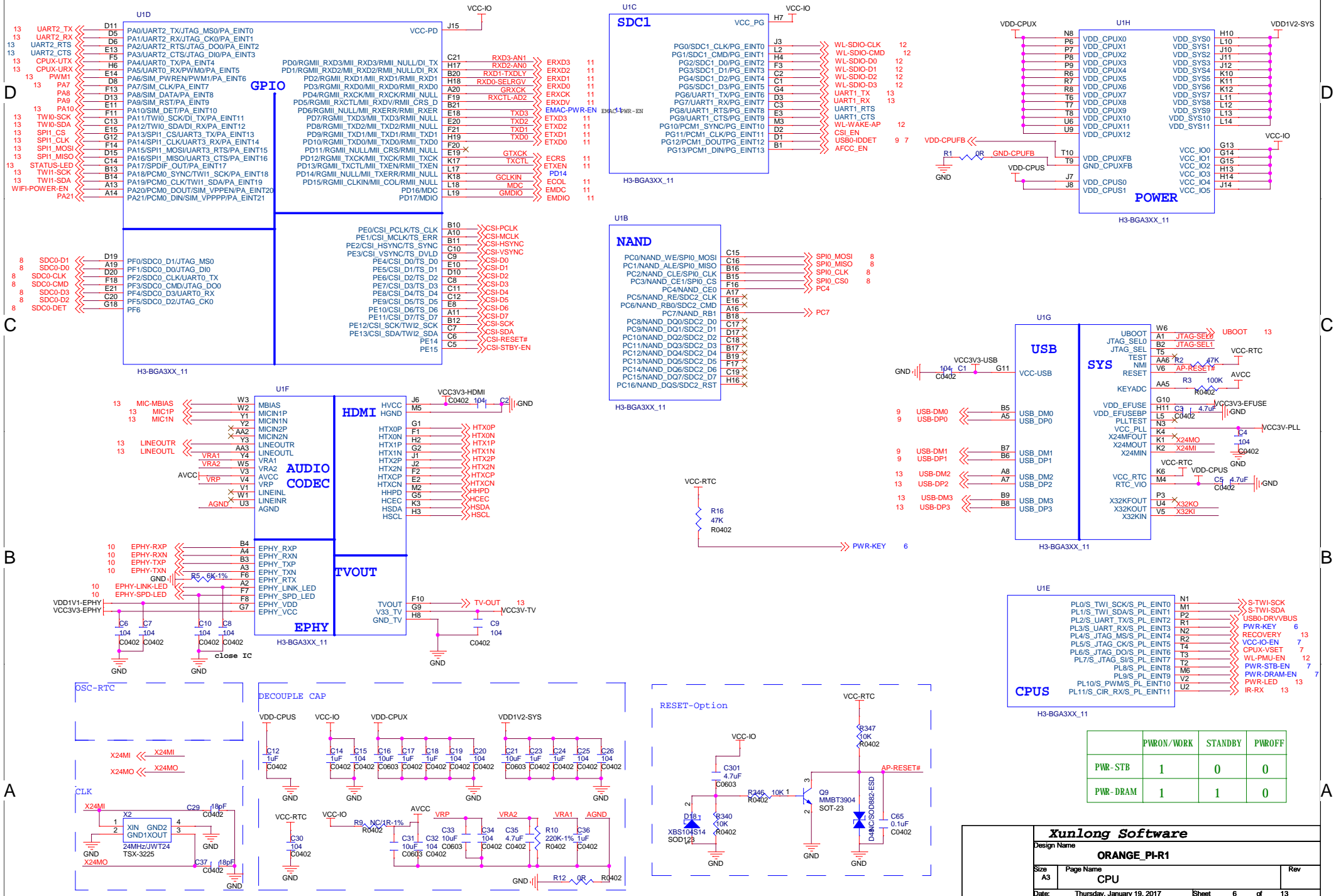
5

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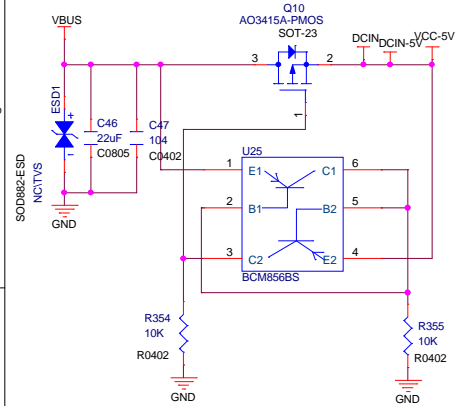
3

2

1



DCIN

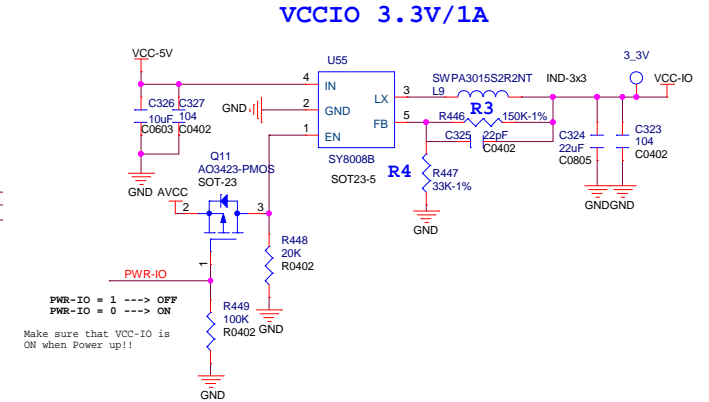
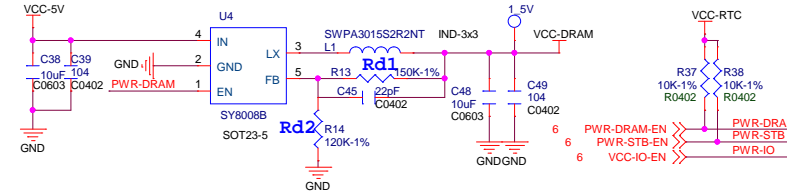


POWER

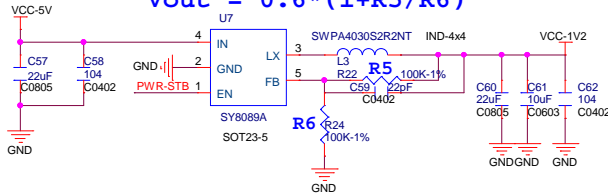
$$V_{out} = 0.6 * (1 + R_{d1}/R_{d2})$$

$$V_{DRAM} = 1.5V/1A, R_2 = 100K-1\%$$

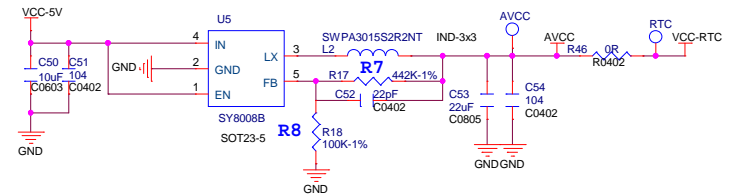
$$V_{DRAM} = 1.35V/1A, R_2 = 120K-1\%$$



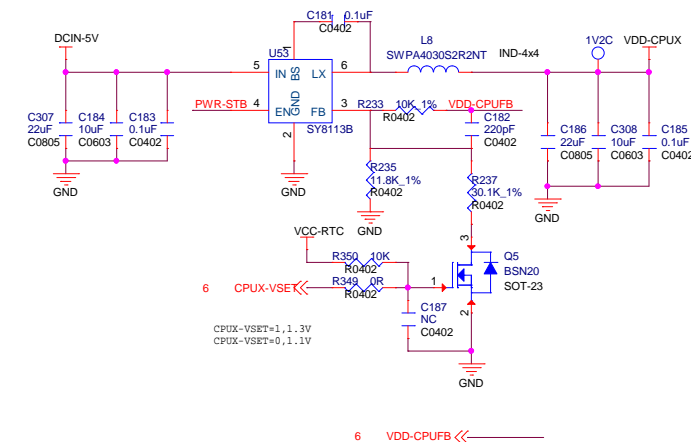
$$V_{out} = 0.6 * (1 + R_5/R_6)$$



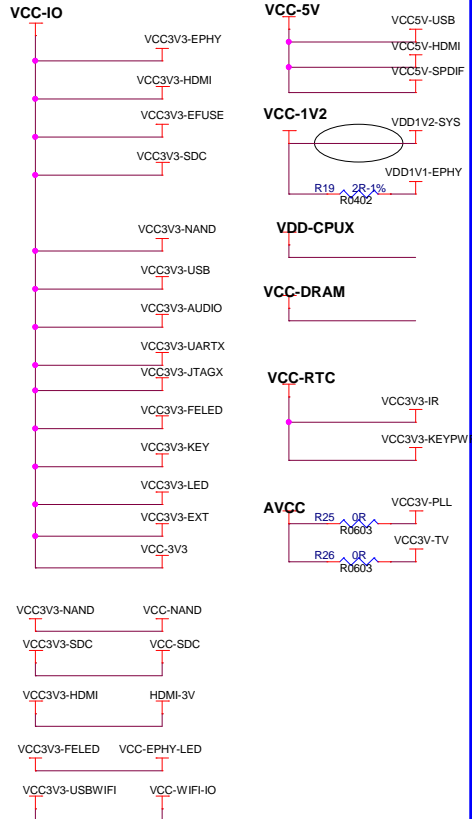
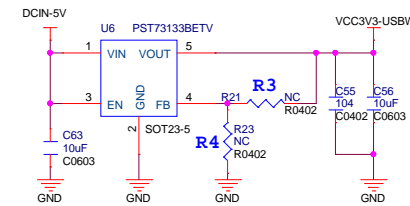
AVCC 3.3V/1A



$$V_{out} = 0.6 * (1 + R_1/R_2)$$



WIFI Power 3.3V/300mA



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Design Name
ORANGE_PI-R1

Size
A3

Page Name
POWER

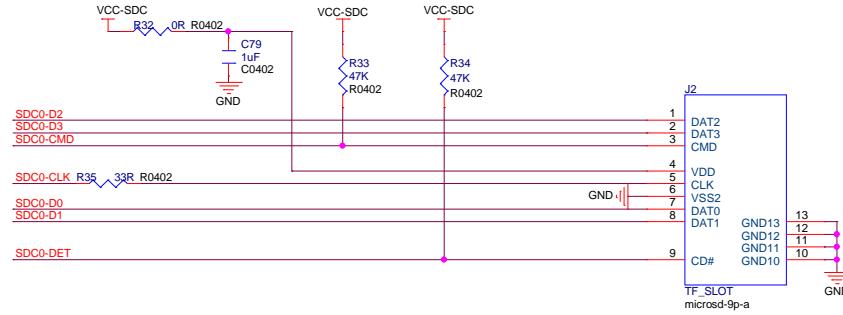
Date
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Sheet
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Rev

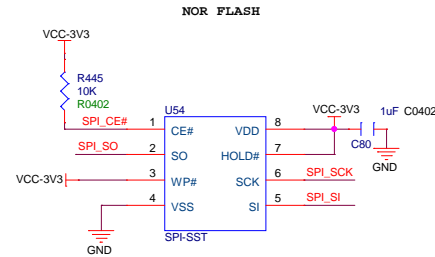
eMMC

6 SDC0-D1
6 SDC0-D0
6 SDC0-CLK
6 SDC0-CMD
6 SDC0-D3
6 SDC0-D2
6 SDC0-DET



NOR FLASH

6 SPI0_MOSI
6 SPI0_MISO
6 SPI0_CLK
6 SPI0_CS0



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USB

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3

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1

D

D

C

C

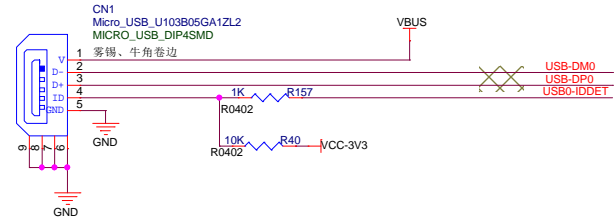
B

B

A

A

6 USB-DM0
6 USB-DP0
6 USB0-IDDET
6 USB0-DRVVBUS



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5 4 3 2 1

EMAC

6 EPHY-RXP
6 EPHY-RXN
6 EPHY-TXP
6 EPHY-TXN
6 EPHY-LINK-LED
6 EPHY-SPD-LED
VCC-EPHY-LED

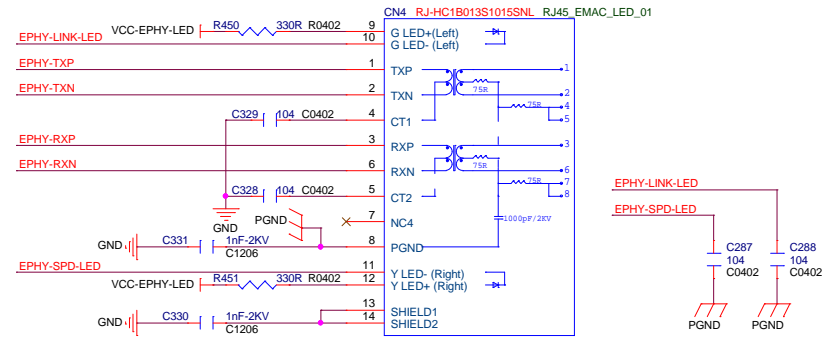
EPHY-LINK-LED VCC-EPHY-LED R450 330R R0402 9
EPHY-TXP 1
EPHY-TXN 2
EPHY-RXP 3
EPHY-RXN 6
GND C331 1nF-2KV C1206 PGND 7
EPHY-SPD-LED VCC-EPHY-LED R451 330R R0402 11
GND C330 1nF-2KV C1206 12
13
14

CN4 RJ-HC1B013S1015SNL RJ45 EMAC_LED_01
G LED+ (Left)
G LED- (Left)
TXP
TXN
CT1
RXP
RXN
CT2
NC4
PGND
Y LED- (Right)
Y LED+ (Right)
SHIELD1
SHIELD2

EPHY-LINK-LED
EPHY-SPD-LED
C287 104 C0402
C288 104 C0402
PGND PGND

10
4
5
6
7
8
104 C0402
104 C0402
1000pF / 20V

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EMAC
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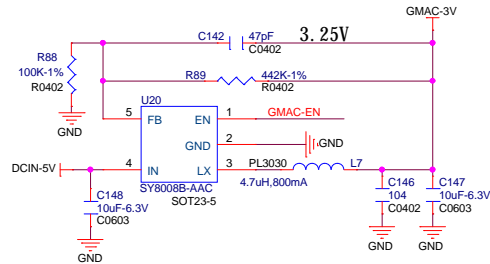
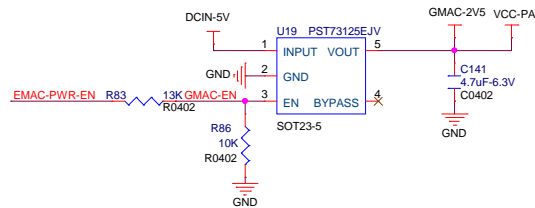
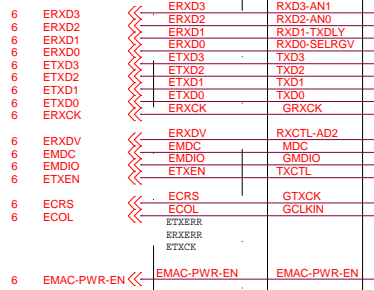


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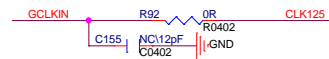
GMAC

10/100/1000 RGMII Ethernet PHY

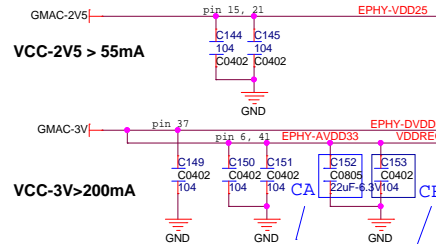
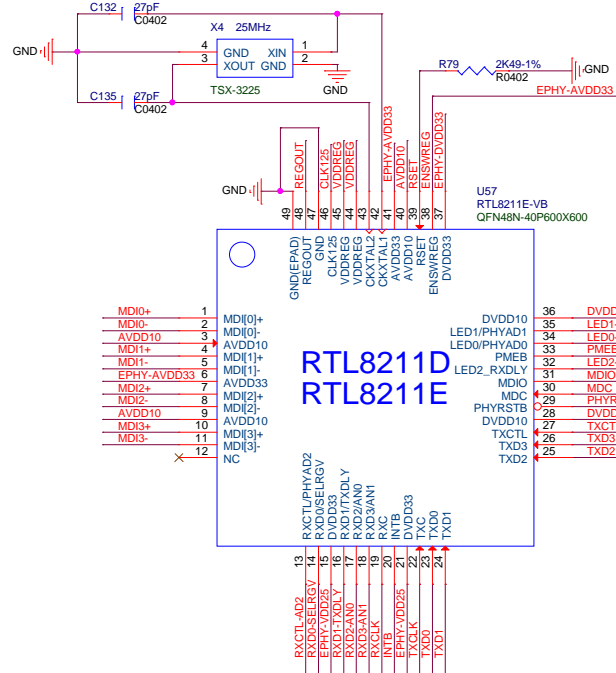
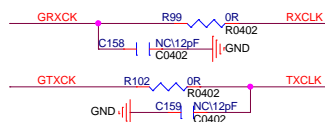
EMAC-MI/GMAC-MI GMAC-RGMII



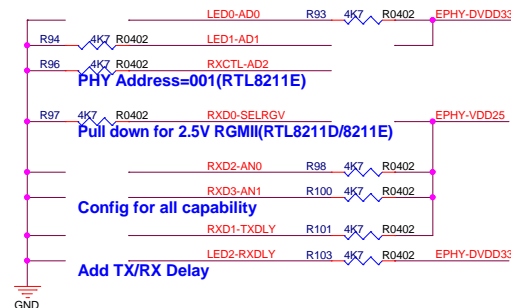
Place filter network close to CLK125.
Reserved for EMI



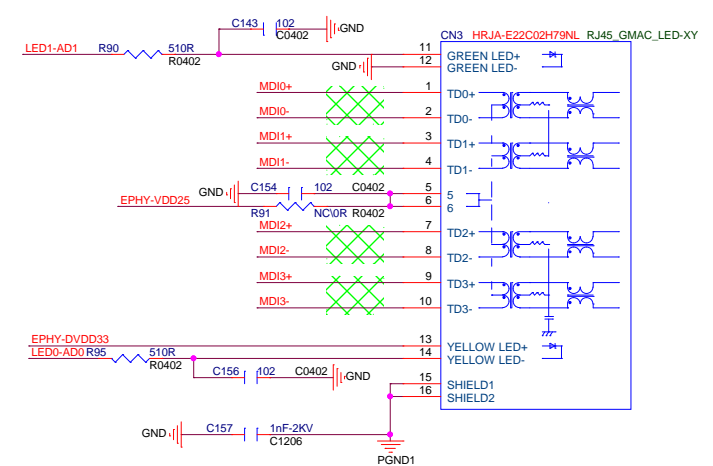
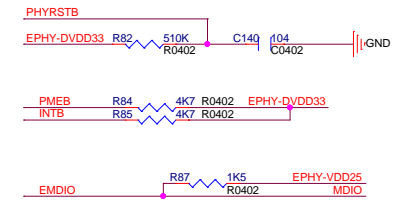
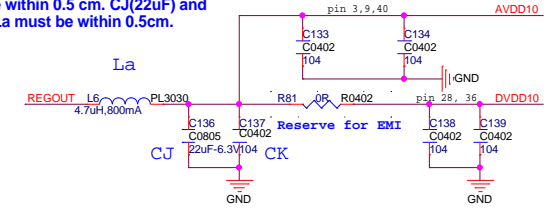
Place filter network close to RX_CLK.
Reserved for EMI



Note 2: The Trace length from CA(22uF),CB(0.1uF) to Pin 44,45(VDDREG) must be within 0.5 cm. The trace width from AVDD33 to Pin 44,45 should be >40mils.



Note 1: The Trace length between La and PHY's Pin48 must be within 0.5 cm. CJ(22uF) and CK(0.1uF) to La must be within 0.5cm.



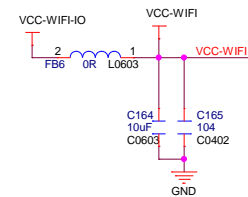
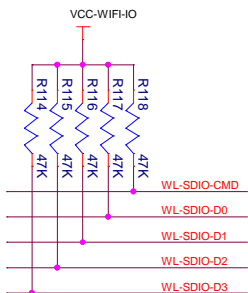
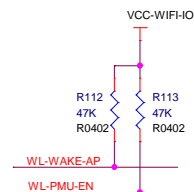
LED0:Blinking=Transmitting or Receiving.
LED1:Link Up/Down

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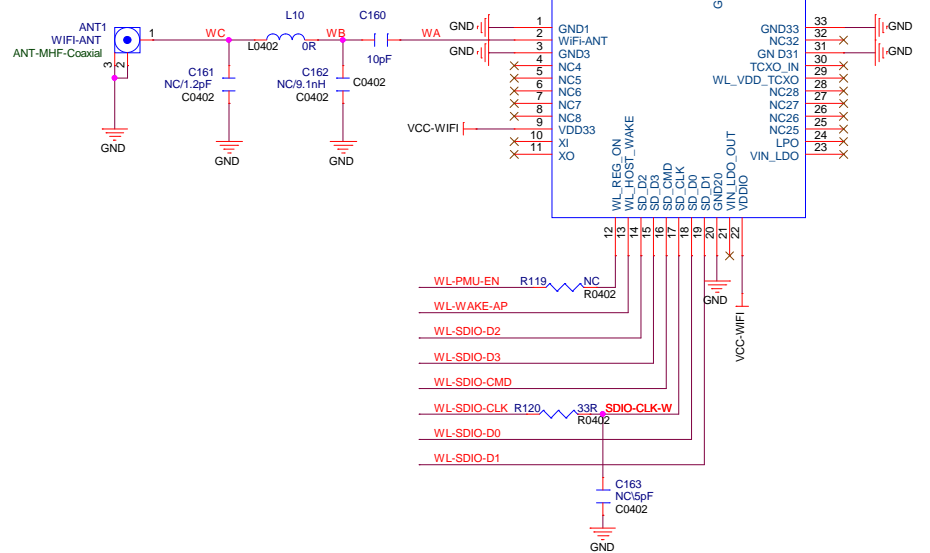
WIFI

6 WL-SDIO-D2
6 WL-SDIO-D3
6 WL-SDIO-CMD
6 WL-SDIO-CLK
6 WL-SDIO-D0
6 WL-SDIO-D1

6 WL-PMU-EN
6 WL-WAKE-AP



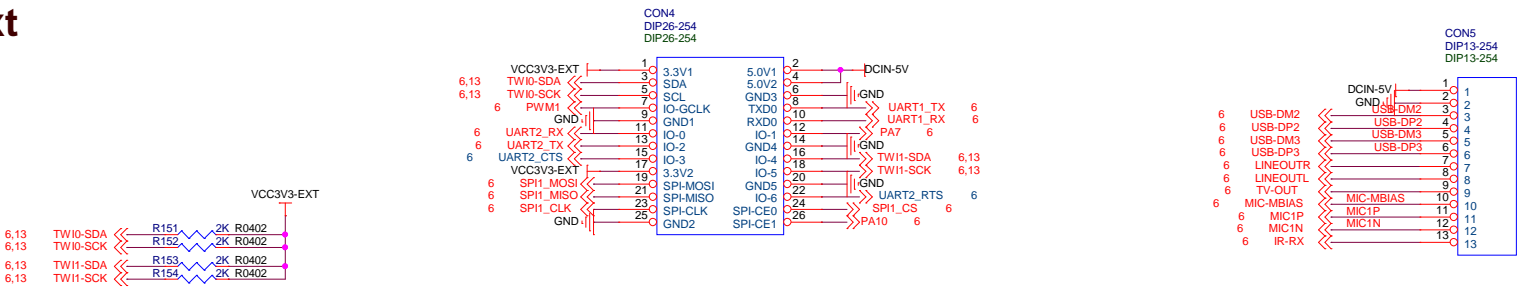
50 Ohm RF trace



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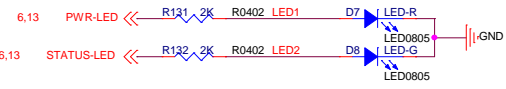
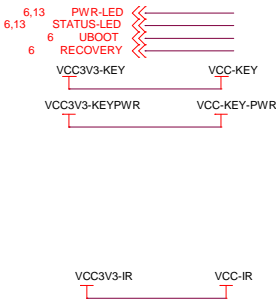
Ext Port

Ext

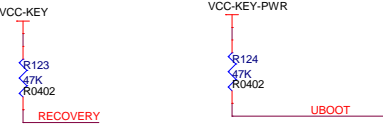


USB*2 @ AUDIO @ IR

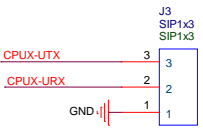
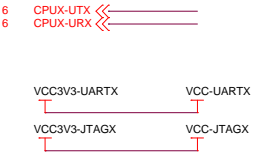
LED



KEY



DEBUG



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